

REMARKS

This Amendment is a full and timely response to the Office Action dated July 5, 2005. Reexamination and reconsideration are respectfully requested.

Priority Acknowledgement

It is noted with appreciation that the Action acknowledged the claim for priority and the submission of certified copies of documents supporting that claim.

Information Disclosure Statement

An Information Disclosure Statement (IDS) accompanies this submission to cite the two documents noted and discussed at pages 1 to 3 in the Description of the Related Art in the specification as filed. An appropriate fee charge is there ordered.

Specification

It was requested in the initial Action that the Applicant's cooperation was requested in correcting any errors of which the Applicant may become aware in the specification. Accordingly, the specification was again reviewed and minor changes made to address minor errors in the text and syntax as shown in the request for an amendment to the specification.

Claims

Claims 1 to 7 were initially rejected as being indefinite, and a minor objection lodged to a spelling incident in claim 1. The latter matter is addressed and corrected along with the amendments provided to pending claims 1 to 7 that are submitted to overcome the indefiniteness rejection.

The applicable law controlling the disposition of rejection made under 35 USC 112 requires that a claim must set out and circumscribe a particular area with a reasonable degree of precision and particularity when read in light of the disclosure as it would be by the artisan. In re Moore, 439 F. 2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971). Acceptability of the claim language depends on whether on of ordinary skill in the art would understand what is claimed in

light of the specification. Seattle Box Co. v. Industrial Crating & Packing, Inc., 731 F. 2d 818, 826, 221 USPQ 568, 574 (Fed. Cir. 1984). It is submitted that no ambiguity or lack of clarity exists in the claim language and it is well settled that the breadth of a claim is not to be equated with indefiniteness. In re Miller, 441 F. 2d 689, 692, 169 USPQ 597, 600 (CCPA 1971). We submit under these standards that the skilled artisan, having considered the specification in its entirety, would have no difficulty ascertaining the scope of the invention recited in claims 1 to 7.

Specifically, claim 1 is amended to avoid the offending use of “the combination of bit information” in favor of a consistent use of a pulse generation circuit for generating a plurality of pulse signals in synchronization with said clock signal (antecedent for which is found in the preamble) and a voltage output circuit having a plurality of coefficient generation circuits for generating a voltage signal proportional to a plurality of different coefficients generated in said coefficient generation circuits in response to said plurality of pulse signals, among other things. Support for the explanations of the coefficient generation circuits is found throughout the specification as filed, it being clear that the coefficient generation circuits generate the plurality of coefficients of an odd number of at least ternary-coefficient-values including a first, a second and a third coefficient, as now claimed. It is submitted that these extended amendments address and overcome any indefiniteness perceived by the examiner in his initial examination.

Claim 2 is amended to conform to claim 1 as amended, even though claim 2 was not rejected as indefinite, thus to provide an antecedent basis for the (n-1) number of ternary-value generation circuits later referred to in claim 3. This provides the clarity sought for original line 4 of claim 3 critiqued by the examiner. The language related to the voltage generation circuit thus is believed to address and overcome any objection as to “the result”, “the maximum” and the sampling points noted in the claim.

Original claims 1 to 7 were rejected as allegedly being anticipated by the JP publication 36109800 to Shiro. The examiner found that the shift register SR acted to generate a plurality of pulse signals using a clock signal C, apparently referring primarily to the English-language Abstract. If the examiner had a translation of the document for use in framing the rejection, a copy is requested.

Shiro generates its pseudo sine curve by generating a succession of positive values,

followed by reversing the polarity of V_{ref} and repeating the cycle to generate negative values. See the sentence spanning the two pages of the English-language abstract.

In contrast, the Applicant's amended claim 1 recites the plurality of coefficient generation circuits generating said plurality of coefficients of an odd number of at least ternary-coefficient-values including a first coefficient, and a second coefficient on the positive side, and a third coefficient at a negative side arranged symmetrically about a center of the first coefficient. See Figs. 1 and 2, for example, noting that the Applicant's arrangement does not require a V_{ref} that is reversed in polarity to generate positive and negative signals in the manner of Shiro. Rather, the SW1 to SWn come into contact with binary values $a_1, -a_1; a_2, -a_2 \dots a_n, -a_n$ for pulse signals S_n, S_3, S_2 and S_1 . See, for example, pages 14 to 17 of the Applicant's specification as filed. It is submitted that the language in amended claim 1 thus avoids anticipation by Shiro.


This distinction is even clearer when considering amended claim 3 that calls for "one binary-value generation circuit for alternately outputting a positive coefficient value and a negative coefficient value in accordance with the control of said pulse signals, among other elements. See also the limitations of amended claims 4, 5, 6 and 7.

The apparatus and the accompanying functional distinctions of amended claims 1 to 7 are clearly distinguished from the apparatus and function of the Shiro publication so that the anticipation rejection of the amended claims should be withdrawn.

Reconsideration of amended claims 1 to 7 is respectfully solicited.

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Respectfully submitted,

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